CLAIMS

1. A wafer, wherein a plurality of strips having a die arrangement structure in which dies are designed to have an equal width are alternately arranged from the center of the wafer.

2. The wafer as claimed in claim 1, wherein first strips positioned closest to the center of the wafer adjoin each other to be symmetric with each other, and other strips arranged sequentially on the outside of the first strips are alternately staggered.

3. The wafer as claimed in claim 1 or 2, wherein the strips comprises:

first strips which have a die arrangement structure in which their dies are designed to have an equal width;

second strips which adjoin the first strips to be symmetric with each other, are arranged in at least one row such that their dies are designed to have an equal width, and are configured in such a manner that their dies are staggered with the respective dies of the first strips;

third strips that adjoin the second strips to be symmetric with each other, are arranged in at least one row such that their dies are designed to have an equal width, and are configured in such a manner that their dies are aligned with those of the first strips but staggered with those of the second strips;

fourth strips that adjoin the third strips to be symmetric with each other, are arranged in at least one row such that their dies are designed to have an equal width, and are configured in such a manner that their dies are aligned with those of the second strips but staggered with those of the first and third strips;

fifth strips that adjoin the fourth strips to be symmetric with each other, are arranged in at least one row such that their dies are designed to have an equal width, and are configured in such a manner that their dies are aligned with those of the first and third strips but staggered with those of the second and fourth strips;

sixth strips that adjoin the fifth strips to be symmetric with each other, are arranged in at least one row such that their dies are designed to have an equal width, and are configured in such a manner that their dies are aligned with those of the second

and fourth strips but staggered with those of the first, third and fifth strips;

seventh strips that adjoin the sixth strips to be symmetric with each other, are arranged in at least one row such that their dies are designed to have an equal width, and are configured in such a manner that their dies are aligned with those of the first, third and fifth strips but staggered with those of the second, fourth and sixth strips;

eighth strips that adjoin the seventh strips to be symmetric with each other, are arranged in at least one row such that their dies are designed to have an equal width, and are configured in such a manner that their dies are aligned with those of the second, fourth and sixth strips but staggered with those of the first, third, fifth and seventh strips; and

ninth strips that adjoin the eighth strips to be symmetric with each other, are arranged in at least one row such that their dies are designed to have an equal width, and are configured in such a manner that their dies are aligned with those of the first, third, fifth and seventh strips but staggered with those of the second, fourth, sixth and eighth strips.

4. The wafer as claimed in claim 3, wherein the first strips are arranged in two rows to be symmetric with each other with respect to the center of the wafer and configured in such a manner that the center of the wafer is located between two specific dies thereof.

5. A method for manufacturing a semiconductor package using a wafer having an alternating arrangement design structure, comprising the steps of:

(1) preparing to saw the wafer (100) by setting the wafer (100) on sawing equipment;

(2) performing a first precise sawing process along a horizontal line (L1) for die design on the wafer (100);

(3) taking away alternately arranged second, fourth, sixth, eighth strips (2, 2'; 4, 4'; 6, 6'; and 8, 8') from the first sawed wafer and moving the second, fourth, sixth and eighth strips so that their vertical lines (L2) for die design are correctly aligned with those of first, third, fifth, seventh and ninth strips;

(4) performing a second precise sawing process along the vertical lines (L2)

for die design of the wafer (100) arranged in the form of a lattice;

(5) singulating the dies (101) attached apiece to an adhesive sheet and mounting the dies on pockets (201) of a carrier (200) one by one;

(6) inspecting reject dies from the carrier (200) mounted with the dies (101);

(7) sorting the reject dies found during the die inspection step and removing the reject dies from the carrier (200);

(8) moving the carrier (200) mounted with only normal dies and supplying the dies (100) to a die bonder (600); and

(9) performing general die bonding process, wire bonding process, molding process and trimming/forming process.

6. The method as claimed in claim 5, wherein the first sawed wafers (100) that have passed through step (2) are moved to a predetermined location so that step (3) can be separately performed at one time.

7. The method as claimed in claim 5, wherein the secondarily sawed wafers (100) that have passed through step (4) are moved to a predetermined location so that step (5) can be separately performed at one time.